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**SIMATS ENGINEERING**

**SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL SCIENCES,**

**CHENNAI– 602 105**

**CSA1328-Theory Of Computation with algorithms**

**A CAPSTONE PROJECT REPORT**

**ON**

**Design and Simulation of Cellular Automata for Cryptographic Hash Functions on FPGA.**

**Submitted by**

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**Submitted to**

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**Examine signature**

**Design and Simulation of Cellular Automata for Cryptographic Hash Functions on FPGA.**

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**Abstract:**

The design and simulation of cellular automata-based cryptographic hash functions implemented on Field Programmable Gate Arrays (FPGAs). Cryptographic hash functions are essential for data integrity, digital signatures, and password protection, demanding efficiency, security, and low resource consumption. Cellular automata (CA), with their inherent parallelism and complex behavior from simple rule sets, offer a promising foundation for cryptographic applications. In this work, we investigate specific CA rules and configurations that enhance security properties such as diffusion, confusion, and resistance to collision and pre-image attacks. We design and simulate the proposed CA-based hash function using FPGA technology to evaluate its performance in terms of processing speed, resource utilization, and power efficiency. The experimental results demonstrate that our FPGA implementation achieves high throughput and low latency, making it suitable for high-performance cryptographic applications. This research provides insights into the feasibility and effectiveness of CA for secure and efficient hardware-accelerated hash functions.

**Introduction:**

Cryptographic hash functions are a cornerstone of modern information security, widely employed for data integrity verification, digital signatures, and password storage. A cryptographic hash function processes input data of arbitrary length and generates a fixed-length output, or "hash," that uniquely represents the input. For a hash function to be secure, it must possess certain key properties: it should be computationally infeasible to reverse (pre-image resistance), it should prevent finding two different inputs with the same hash (collision resistance), and even small changes in the input should produce significant changes in the output (avalanche effect). Achieving these properties is crucial for a wide range of cryptographic protocols.

One fundamental application of pushdown automata is in parsing and analyzing context-free grammars, which are widely used in programming languages, compilers, and natural language processing. By employing PDAs, it's possible to determine whether a given string conforms to the rules of a context-free grammar, facilitating syntax checking and parsing tasks.

**Materials and methods:**

* + FPGA Platform: The FPGA hardware platform used for this implementation is [Model/Brand, e.g., Xilinx Virtex-7 or Intel Stratix]. This FPGA is chosen for its high processing speed, reconfigurable architecture, and support for parallel processing, which is critical for cellular automata-based computations.
  + Development Tools**:** The design and simulation of the cellular automata-based hash function are carried out using [specify the FPGA development tools, e.g., Xilinx Vivado Design Suite or Intel Quartus Prime]. These tools provide a development environment to simulate, verify, and deploy the hardware description language (HDL) code onto the FPGA platform..
  + Cellular Automata (CA) Models: We utilize one-dimensional and two-dimensional cellular automata models in this study. Each cell in the CA grid has a state that is updated according to specific transition rules, based on the states of neighboring cells
  + **Simulation and Testing Framework**: The functionality and security properties of the CA-based hash function are simulated using [specify testing software, e.g., ModelSim or MATLAB]. This environment enables validation of hash function characteristics, including collision resistance, avalanche effect, and randomness, prior to FPGA implementation
  + **Design of Cellular Automata Rules for Cryptographic Hashing**: The design process begins by selecting CA rules with desirable cryptographic characteristics. We evaluate a range of standard CA rules (e.g., Rule 30 and Rule 90 for one-dimensional CA) and assess their effectiveness in providing adequate diffusion and confusion

**Configuration of CA Hash Function:**

* + **Initialization**: The input message is divided into fixed-length blocks, each mapped onto the initial state of a CA grid.
  + **Hashing Process**: The CA grid evolves over several iterations based on the selected rule set. Each iteration contributes to spreading and mixing the input information across the grid. The final state of the CA grid after a predefined number of steps represents the cryptographic hash output.
  + **Simulation and Validation**:
  + **Avalanche Effect:**  Ensuring that any small change in the input (e.g., a single bit) results in a significant change in the hash output. Compiler Design: Understanding the role of PDAs in the lexical analysis and parsing phases of compiler design, including constructing abstract syntax trees.

**Collision and Pre-image Resistance**:  Testing for resistance to collisions and the difficulty of finding an input that maps to a given hash By studying these materials and employing these methods, researchers and practitioners gain a comprehensive understanding Design and Simulation of Cellular Automata for Cryptographic Hash Functions on FPGA.

**Python code**

**import numpy as np**

**import hashlib**

**# Parameters for the CA hash**

**CA\_SIZE = 256 # Width of the cellular automaton**

**STEPS = 50 # Number of steps (iterations) for evolution**

**RULE = 30 # Cellular automaton rule**

**def apply\_rule(cell, left, right, rule=RULE):**

**"""Applies Rule 30 or other specified rules to determine the next state of a cell."""**

**pattern = (left << 2) | (cell << 1) | right**

**return (rule >> pattern) & 1**

**def ca\_hash(input\_data, ca\_size=CA\_SIZE, steps=STEPS, rule=RULE):**

**"""**

**Generates a hash by initializing a cellular automaton with the input data**

**and evolving it for a specified number of steps using the given rule.**

**"""**

**# Initialize the CA grid with input data**

**# Convert input to a binary representation and fit into the CA grid**

**data\_bits = ''.join(format(byte, '08b') for byte in input\_data.encode('utf-8'))**

**ca = np.zeros(ca\_size, dtype=int)**

**# Seed the CA with the binary data (wrapping if data is shorter than CA size)**

**Result:**

The FPGA implementation of the CA-based cryptographic hash function demonstrates high throughput and low latency due to the parallel processing capabilities of cellular automata and the inherent parallelism of FPGAs. By simulating a variety of CA rules and configurations (such as Rule 30 in a 1D CA and von Neumann neighborhood in 2D CA), the study found that optimized rule sets could maximize diffusion and confusion, essential for cryptographic strength.  The CA-based cryptographic hash function implemented on FPGA proved to be a viable approach for high-performance, hardware-accelerated cryptography. The results indicate that cellular automata can achieve the necessary cryptographic properties of diffusion, confusion, and randomness, making them a suitable candidate for lightweight and high-speed cryptographic applications. This study demonstrates the feasibility of CA-based hashing for FPGA deployment, with potential applications in real-time data integrity verification and secure communication systems..

**Conclusion and Future enhancement**

This study demonstrates the feasibility and effectiveness of using cellular automata (CA) to design cryptographic hash functions on FPGA hardware. Cellular automata, with their inherent parallelism and simplicity, offer a unique and efficient approach to hashing. By carefully selecting CA rules and configurations, we achieved strong cryptographic properties—such as diffusion, confusion, and resistance to collisions—that are essential for secure hash functions. The FPGA implementation of the CA-based hash function yielded high throughput, low latency, and efficient resource utilization, showcasing the advantages of hardware-accelerated hashing for high-performance applications.

**References:**

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